REMARKS

The Examiner's Action mailed on September 14, 2006 has been received and its contents have been carefully considered.

In this Amendment, Applicants have amended claims 1 and 9 to correct minor typographical errors. Claims 17-21 are added to further protect the invention. Claims 1, 9, and 17 are the independent claims. Claims 1-21 are now pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

Claims 1 and 9 are objected to because of informalities as set forth in the Office Action. In response, claims 1 and 9 have been corrected as required. Withdrawal of the objection is respectfully requested.

Claims 1, 4-9 and 12-16 have been rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over the Applicant's Admitted Prior Art (*AAPA*) (Fig. 1A) in view of *Tomobe et al.* (U.S. Patent No. 6,198,334). It is submitted that these claims patentably distinguish the invention over the cited reference for at least the following reasons.

It is well settled that cited references would render a claim at issue obvious within the purview of 35 U.S.C. §103 only if there is suggestion or motivation in the prior art to combine or modify the cited references to arrive at all the features and all the relationships recited in the claim. In particular, "[p]atentability shall not be negatived by the manner in which the invention was made." However, the cited references do not disclose, or do they even suggest, all the features and relationships recited in independent claims 1 and 9.

Independent claim 1 recites **a phase-interpolation circuit** for outputting a third clock signal according to **a first clock signal and a second clock signal**. **The phase-interpolation circuit** comprises **a first inverter** for receiving **the first clock signal**, **a second inverter** for receiving **the second clock signal**, **a first controlled switch coupled to the first inverter, the second inverter, and a power source**, and **a second controlled switch coupled to the first inverter, the second inverter, and ground**. An output end of the second inverter is coupled to an output end of the first inverter to form a common output end to output the third clock signal. **The first controlled switch** is "off" when **the first clock signal** is in a first state, and is "on" when **the first clock signal** is in a second state. **The second controlled switch** is "on" when **the first clock signal** is in the first state, and is "off" when **the first clock signal** is in the second state. The phase of the third clock signal is determined by the phase of the first clock signal and the second clock signal. In addition, similar structural features are also recited in Independent claim 9. Due to the structural and other features of the **phase-interpolation circuit**, as recited in claim 1 or 9, **a short-circuit current of the phase-interpolation circuit is avoided**.

However, in contrast to the structure of Applicants' invention as defined in claim 1 or 9, *AAPA* in Fig. 1A, relied on by the Office Action, discloses, among four other conventional examples, a phase interpolation circuit merely composed of two inverters. The Office Action acknowledges that the *AAPA* (Fig. 1A) does not disclose a detailed configuration of inverters as recited in the Applicants' claims, including, among the others, **a first controlled switch coupled to the first inverter, the second inverter, and a power source, wherein the first**

controlled switch being "off" when the first clock signal is in a first state, and being "on" when the first clock signal is in a second state; and **a second controlled switch coupled to the first inverter, the second inverter, and ground, wherein the second controlled switch being "on" when the first clock signal is in the first state, and being "off" when the first clock signal is in the second state**.

To resolve the deficiencies of the *AAPA*, the Office Action points to *Tomobe et al.* as disclosing a detailed configuration of a CMOS inverter circuit (in Figure 1) and a truth table for the CMOS inverter circuit operation (in Figure 5). The Office Action asserts that the CMOS inverter circuit of *Tomobe et al.* in Figure 1 comprises (1) an input end [INPUT TERMINAL], (2) a first controlled switch [P1], (3) a CMOS inverter [P2, N2], and (4) a second controlled switch [N1]; wherein all [P1, P2, N1, N2] are connected in series.

In addition, the Office Action asserts

> [t]o modify the phase interpolation circuit of the Applicant's Admitted Prior Art (Fig. 1A) by configuring in the CMOS inverters of the Applicant's Admitted Prior Art (Fig. 1A) with the PMOS and NMOS transistors connected in series in each inverter to cause switching speeds of the transistors and thus to improve the noise resistance performance of the phase interpolation circuit would have been obvious to one of ordinary skills in the art at the time of the invention since such a configuration of the PMOS and NMOS transistors in the CMOS inverters for the stated purpose has been a well-known practice in the art as evidenced by the teachings of *Tomobe et al.* (see *Tomobe et al.*; Abstract, lines 1-7).

However, it is submitted that these assertions do not resolve the deficiencies of the *AAPA*, since *Tomobe et al.*do not disclose or even suggest all the structure and the relationship of features of the rejected claim that are missing from *AAPA*, as explained below.

First, the disclosure of *Tomobe et al.* is directed to a CMOS noise eliminating circuit, and FIG. 1 of this reference discloses a CMOS inverter circuit for receiving **an input signal** at "INPUT TERMINAL" and outputting an output signal at "OUTPUT TERMINAL." In contrast to a phase interpolation circuit of the invention that receives at least **two input signals**, the illustrated inverter circuit of the reference with **only one input terminal for an input signal**, as well as related descriptive passages (col. 4, line 11 to col. 5, line 42), fails to disclose or even suggest a structure of the phase interpolation, as recited in independent claims 1 and 9. What *Tomobe et al.* discloses in Figure 1, as well as the related passages, is to provide a CMOS inverter circuit as shown in Figure 1 in place of a conventional CMOS inverter circuit composed of a PMOS transistor and an NMOS transistor, as shown in FIG. 10(A), so that **the false operation due to noise induced in the input signal** of the inverter circuit will not occur.

Second, it is noted that the truth table shown in FIG. 5 of *Tomobe et al.* is for a third embodiment of the CMOS noise eliminating circuit shown in FIG. 4(A) and FIG. 4(B) (see col. 5, lines 25-45), not for the CMOS inverter circuit shown in FIG. 1. The circuit shown in FIG. 4(A) does not disclose or even suggest a phase interpolation circuit, but rather discloses a 2-input NAND logical gate for the similar purpose of noise elimination.

Thus, *Tomobe et al.* actually do not mention phase interpolation, since this reference merely directs one of ordinary skill in the art to solving the problem of the false operation due to **noise induced into the input signal of the inverter circuit** (see col. 1, lines 29-43; FIGs. 10(A), 10(B), 11-13 of *Tomobe et al.*). By contrast, FIG. 1 of *Tomobe et al.*, as well as FIG. 4(A), do not disclose or even

suggest **a phase interpolation circuit** for outputting a third clock signal according to **a first clock signal and a second clock signal,** comprising, among others, **a first controlled switch and a second controlled switch wherein** (1) **the first controlled switch** is coupled to **a first inverter, a second inverter, and a power source**; (2) **the second controlled switch** is coupled to **the first inverter, the second inverter, and ground**; **while** (3) the state of the **first clock signal determines the states** of being **"on" or "off" of the first controlled switch and the second controlled switch**, as required by each of claims 1 and 9. Accordingly, these structural and other features as indicated by (1), (2), and (3) above are missing from *AAPA* and are neither disclosed nor even suggested by *Tomobe et al.*

In addition, no disclosure or suggestion is provided to one of ordinary skill in the art at the time of the invention to **specifically select one of four examples of the *AAPA*** and **combine such a selected one** and **a reference which does not mention phase interpolation**, i.e. *Tomobe et al.*, to arrive at all the structure and all relationship of features recited in these claims.

As such, it is respectfully submitted that the structure of claims 1 and 9 is not rendered obvious by *AAPA* and *Tomobe et al.*, whether taken alone or in combination. For at least this reason, it is respectfully submitted that claims 1 and 9, as well as their respective dependent claims 4-8 and 13-16, are clearly patentable over the cited references, and the rejection of these claims accordingly should be withdrawn.

As a further basis for patentability of independent claims 1 and 9, Applicants respectfully submit that there is no suggestion and motivation to

combine the *AAPA* and *Tomobe et al.*, as proposed by the Office Action to arrive at all feature and relationships of the claims rejected.

In determining obviousness, it is impermissible to pick and choose from any one reference only so much as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art.

In this regard, the Office Action asserts that:

> [t]o **modify the phase interpolation circuit of the Applicant's Admitted Prior Art (Fig. 1A) by configuring in the CMOS inverters of the Applicant's Admitted Prior Art (Fig. 1A) with the PMOS and NMOS transistors connected in series in each inverter** to cause switching speeds of the transistors and thus to improve the noise resistance performance of the phase interpolation circuit **would have been obvious** to one of ordinary skills in the art at the time of the invention **since such a configuration** of the PMOS and NMOS transistors in the CMOS inverters for the stated purpose **has been a well-known practice** in the art as evidenced by the teachings of *Tomobe et al.* (*emphasis added*)

Applicants respectfully disagree with this assertion and submit that such reasons for combination of the *AAPA* and *Tomobe et al.* constitute merely a conclusory statement that is insufficient to explain how one of ordinary skill in the art would have been motivated to make such a combination to arrive at the claim rejected. That is:

First, the *AAPA* discloses four examples of phase interpolation circuits (see FIGS. 1A, 1B, 1D, and 2A). The *AAPA* discloses that the phase interpolation circuit shown in FIG. 1A has various disadvantages including a short-circuit current problem (see paragraph [0007]), and an improved prior art circuit in FIG. 1D is provided to solve some of the problems in the circuit of FIG. 1A (see paragraph [0008]).

Second, as above discussed, *Tomobe et al.* is irrelevant to phase interpolation and provides no phase interpolation circuit, and the CMOS inverter circuit shown in its FIG. 1 is merely an inverter that does not disclose the structural features and relationships recited in the rejected claim that are missing from *AAPA*.

In view of the teaching from the *AAPA* and *Tomobe et al.*, one would question how one having ordinary skill in the art would have been motivated to **specifically select FIG. 1A of the four examples of the *AAPA* as a basis, and combine such specifically selected basis** with **a reference which does not mention phase interpolation, namely *Tomobe et al.*** One also may question how the references were combined, and how they would operate to arrive at all the structure and all relationship of features recited in the claims. However, the Office Action appears to ignore these issues. Rather, the Office Action provides merely a conclusory statement that

> "**[t]o modify the phase interpolation circuit of the Applicant's Admitted Prior Art (Fig. 1A) by configuring in the CMOS inverters of the Applicant's Admitted Prior Art (Fig. 1A) with the PMOS and NMOS transistors connected in series in each inverter ... would have been obvious** to one of ordinary skills in the art at the time of the invention **since such a configuration ... has been a well-known practice** in the art as evidenced by the teachings of *Tomobe et al.*" (*emphasis added*)

Accordingly, Applicants respectfully assert that the argument in the Office Action is a classic example of impermissible hindsight reasoning and, in particular, has pointed to no teaching within the references that relates the desirability of combining the selected features. As discussed above, it is the prior art which must properly suggest the desirability of combining the particular elements, for it is axiomatic that all elements and features are taught somewhere in the prior art.

Thus, for at least these reasons, as a matter of law, the rejections of claims 1 and 9, as well as dependent claims 4-8 and 12-16 are improper and should be withdrawn.

Claims 2-3 and 10-11 have been rejected under 35 U.S.C. §103(a) as being unpatentable over the *AAPA* (Fig. 1A) in view of *Tomobe et al.* (U.S. Patent No. 6,198,334) as applied to claims 1 and 9 above, and further in view of *Kim* (U.S. Patent No. 6,225,847). It is submitted that these claims are patentably distinguishable over the cited reference for at least the following reasons.

Claims 2-3 and 10-11 depend from independent claims 1 and 9, respectively. *Kim* is directed to complementary clock generator and method for generating complementary clocks. *Kim* fails to disclose or even suggest all features and relationships recited in either of claims 1 and 9 that are missing from the *AAPA* and *Tomobe et al.* In addition, there is no disclosure or suggestion to one of ordinary skill in the art to combine the three references to arrive at all features of the claims rejected. Claims 2-3 and 10-11 are thus deemed clearly to be patentably over the cited references at least for the reasons advanced above as to the patentability of independent claims 1 and 9, and for the additional features they recite that are missing from the teachings of the *AAPA* and *Tomobe et al.*

Further, new claims 17-21 are added to further protect the invention, and are patentably at least for reasons similar to those advanced above as to claims 1-16. Moreover, it is submitted that no new matter is added in these new claims.

Conclusion

Accordingly, it is submitted that all of the pending claims are allowable over the cited references, so that this application is in condition for allowance. Such action and the passing of this case to issue are therefore respectfully requested.

If the Examiner believes that a conference would be of value in expediting the prosecution of this application, the Examiner is hereby invited to telephone the undersigned counsel to arrange for such a conference.

A fee in the amount of $500.00 is attached in payment of the two-month extension of time fee, $450.00, and additional claims fee of $50.00 (one excess claim), by way of credit card payment form (Form PTO-2038). Should the remittance be accidentally missing or insufficient, however, the Commissioner is hereby authorized to charge the fee to our Deposit Account No. 18-0002, and advise us accordingly.

Respectfully submitted,

February 14, 2007
Date

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